AMENDMENTS

In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently amended) A method to form a transistor gate in the manufacture of an integrated circuit device, said method comprising:

providing a substrate;

forming a conductor layer overlying said substrate with a dielectric layer therebetween;

forming a masking layer overlying said conductor layer;

forming a resist layer overlying said masking layer;

patterning said resist layer to thereby selectively expose said masking layer wherein said resist layer exhibits a first spacing between edges of said resist layer;

etching through said exposed masking layer to thereby selectively expose said conductor layer wherein etched edges of said masking layer are tapered and the angle of the edges of said masking layer with respect to the top surface of said substrate is between about 45° and about 85° such that said masking layer exhibits a second spacing between said masking layer edges at the top surface of

said conductor layer and wherein said second spacing is less than said first spacing; and

etching through said exposed conductor layer to thereby complete a transistor gate.

Claim 2 (Original) The method according to claim 1 wherein said conductor layer comprises polysilicon.

Claim 3 (Original) The method according to claim 1 wherein said masking layer comprising silicon nitride.

Claim 4 (Original) The method according to claim 1 wherein said step of etching through said exposed masking layer comprising a dry etch further comprising an etching chemistry of CFH_3, CF_4, O_2, and He.

Claim 5 (Cancelled)

Claim 6 (Original) The method according to claim 1 wherein said masking layer comprising a thickness of between about 600 Å and about 4,000 Å.

Claim 7 (Original) The method according to claim 1 further comprising forming an isolation region in said substrate wherein said masking layer etched edges overlies said isolation region.

Claim 8 (Original) The method according to claim 1 wherein said transistor gate is a floating gate of a non-volatile memory device.

Claim 9 (Original) The method according to claim 8 further comprising:

forming a control gate overlying said floating gate wherein said control gate comprises a second conductor layer overlying a second dielectric layer; and

forming source and drain regions in said substrate.

Claim 10 (Original) A method to form floating gate of a non-volatile memory device, said method comprising:

providing a substrate;

forming an isolation region in said substrate;

forming a conductor layer overlying said substrate with a dielectric layer therebetween;

forming a masking layer overlying said conductor layer;

forming a resist layer overlying said masking layer;

patterning said resist layer to thereby selectively expose said masking layer wherein said resist layer exhibits a first spacing between edges of said resist layer;

etching through said exposed masking layer to thereby selectively expose said conductor layer wherein etched edges of said masking layer are tapered such that said masking layer exhibits a second spacing between said masking layer edges at the top surface of said conductor layer and wherein said second spacing is less than said first spacing and wherein said masking layer etched edges overlies said isolation region; and

etching through said exposed conductor layer to thereby complete a floating gate of a non-volatile memory device.

Claim 11 (Original) The method according to claim 10 wherein said conductor layer comprises polysilicon.

Claim 12 (Original) The method according to claim 10 wherein said masking layer comprising silicon nitride.

Claim 13 (Original) The method according to claim 10 wherein said step of etching through said exposed masking layer comprising a dry etch further comprising an etching chemistry of CFH_3, CF_4, O_2, and He.

Claim 14 (Original) The method according to claim 10 wherein the angle of the edges of said masking layer with respect to the top surface of said substrate is between about 45° and about 85°.

Claim 15 (Original) The method according to claim 10 wherein said masking layer comprising a thickness of between about 600 Å and about 4,000 Å.

Claim 16 (Original) The method according to claim 10 further comprising:

forming a control gate overlying said floating gate wherein said control gate comprises a second conductor layer overlying a second dielectric layer; and

forming source and drain regions in said substrate.

Claim 17 (Original) A method to form floating gate of a non-volatile memory device, said method comprising:

providing a substrate;

forming a shallow trench isolation in said substrate;

forming a polysilicon layer overlying said substrate with a dielectric layer therebetween;

forming a masking layer overlying said polysilicon layer;

forming a resist layer overlying said masking layer;

patterning said resist layer to thereby selectively expose said masking layer wherein said resist layer exhibits a first spacing between edges of said resist layer;

etching through said exposed masking layer to thereby selectively expose said polysilicon layer wherein etched edges of said masking layer are tapered such that said masking layer exhibits a second spacing between said masking layer edges at the top surface of said polysilicon layer and wherein said second spacing is less than said first spacing and wherein said masking layer etched edges overlies said isolation region;

etching through said exposed polysilicon layer to thereby complete a floating gate;

forming a control gate overlying said floating gate wherein said control gate comprises a second conductor layer overlying a second dielectric layer; and

forming source and drain regions in said substrate to complete a non-volatile device.

Claim 18 (Original) The method according to claim 17 wherein said step of etching through said exposed masking layer comprising a dry etch further comprising an etching chemistry of CFH_3, CF_4, O_2, and He.

Claim 19 (Original) The method according to claim 17 wherein the angle of the edges of said masking layer with respect to the top surface of said substrate is between 45° and about 85°.

Claim 20 (Original) The method according to claim 17 wherein said masking layer comprising a thickness of between about 600 Å and about 4,000 Å.